



FIG. 1

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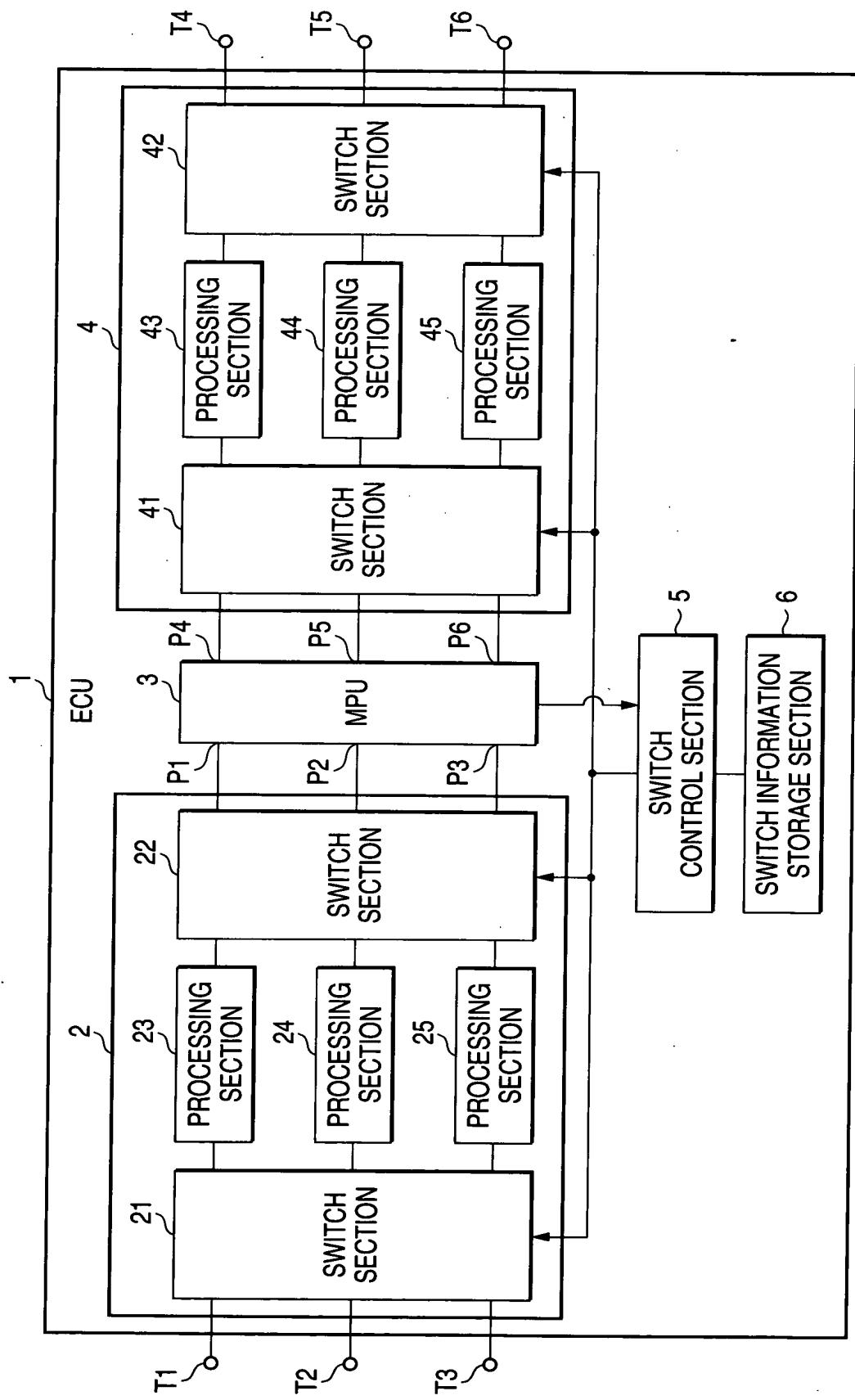


FIG. 2

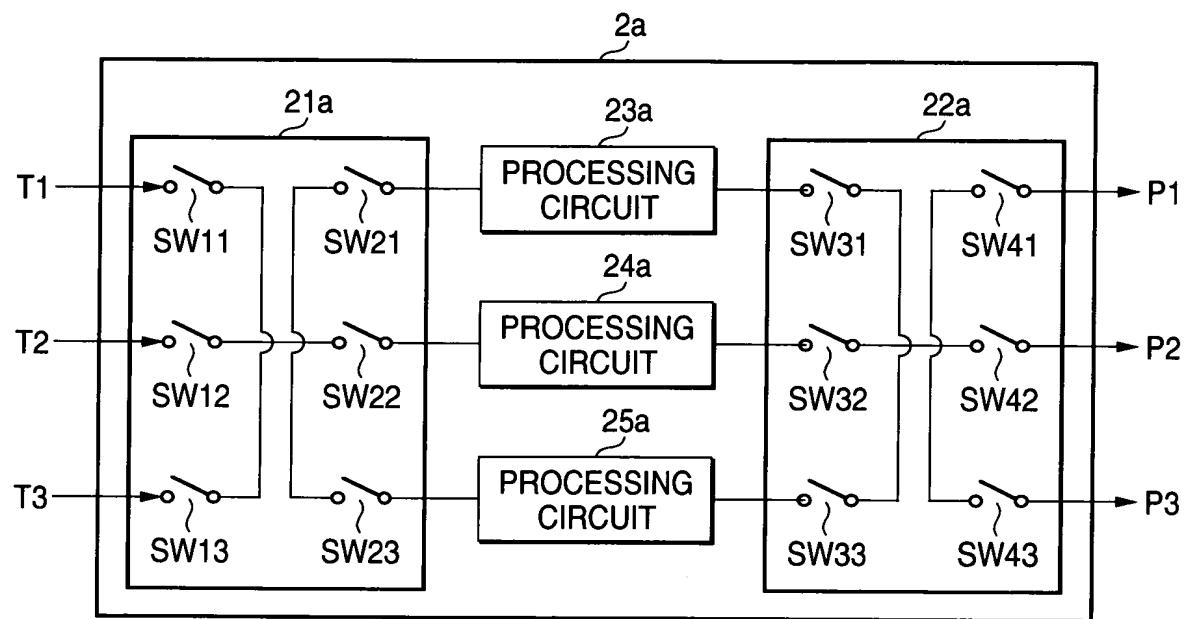


FIG. 3 (a)

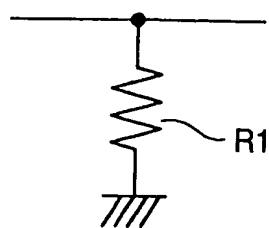


FIG. 3 (b)

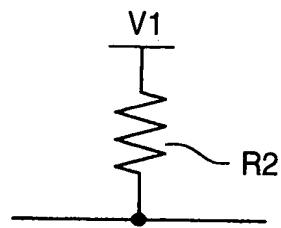


FIG. 3 (c)

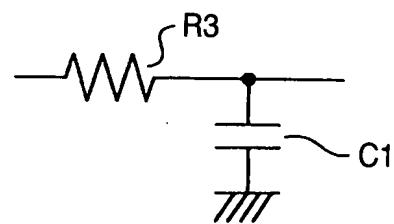


FIG. 3 (d)

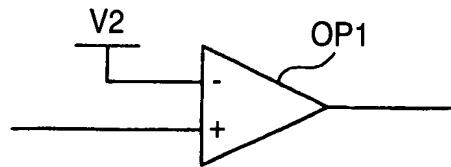


FIG. 4 (a)

INPUT TERMINAL T1	PROCESSING A	INPUT PORT P2
INPUT TERMINAL T2	PROCESSING B	INPUT PORT P3
INPUT TERMINAL T3	PROCESSING C	INPUT PORT P1

FIG. 4 (b)

INPUT TERMINAL T1	SWITCH S11	SWITCH S21	SWITCH S31	SWITCH S42
INPUT TERMINAL T2	SWITCH S12	SWITCH S22	SWITCH S32	SWITCH S43
INPUT TERMINAL T3	SWITCH S13	SWITCH S23	SWITCH S33	SWITCH S41

FIG. 5 (a)

INPUT TERMINAL T1	PROCESSING B	INPUT PORT P2
INPUT TERMINAL T2	PROCESSING A	INPUT PORT P3
INPUT TERMINAL T3	PROCESSING C	INPUT PORT P1

FIG. 5 (b)

INPUT TERMINAL T1	SWITCH S11	SWITCH S22	SWITCH S32	SWITCH S42
INPUT TERMINAL T2	SWITCH S12	SWITCH S21	SWITCH S31	SWITCH S43
INPUT TERMINAL T3	SWITCH S13	SWITCH S23	SWITCH S33	SWITCH S41

FIG. 6

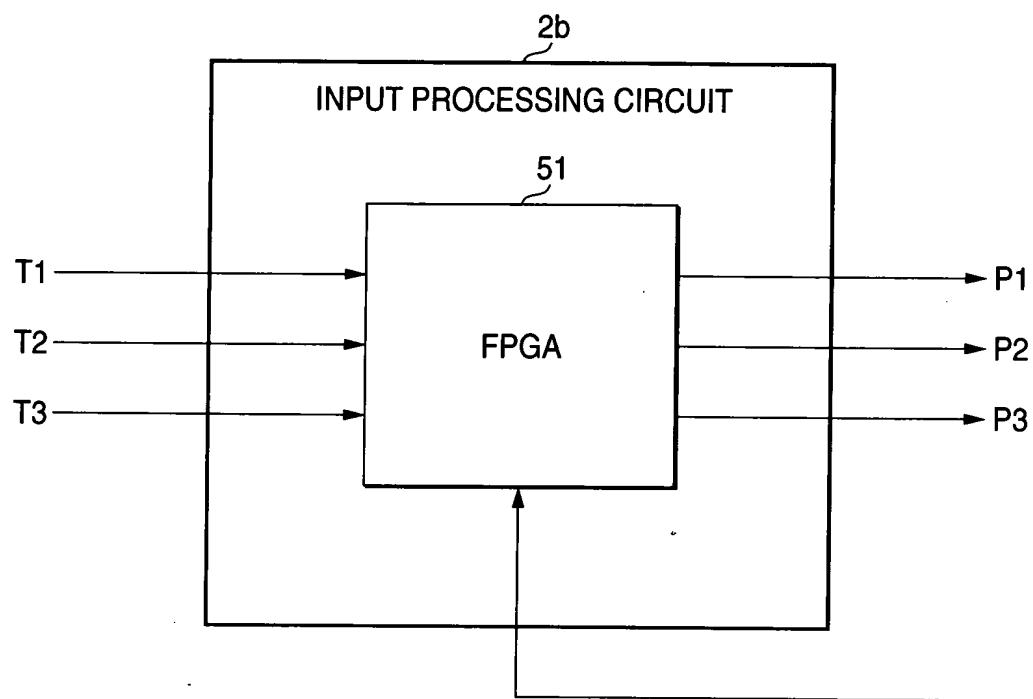


FIG. 7

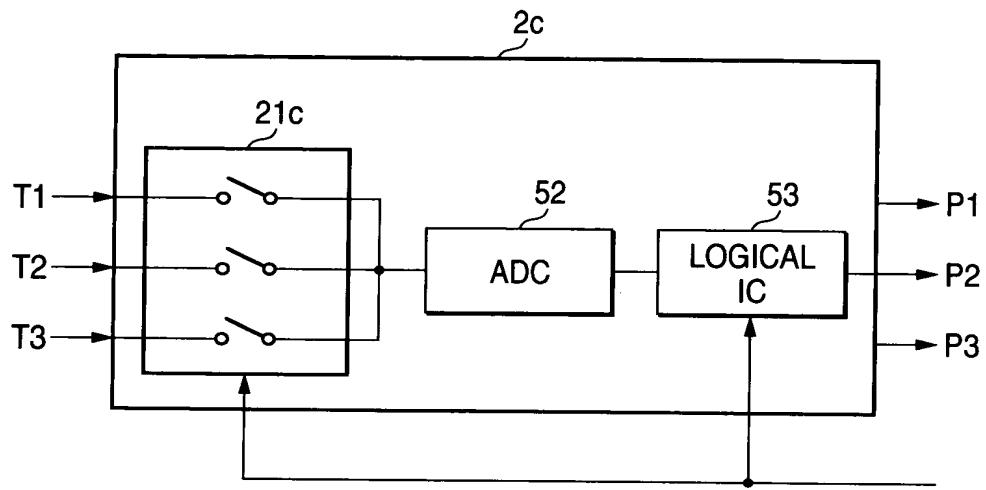


FIG. 8

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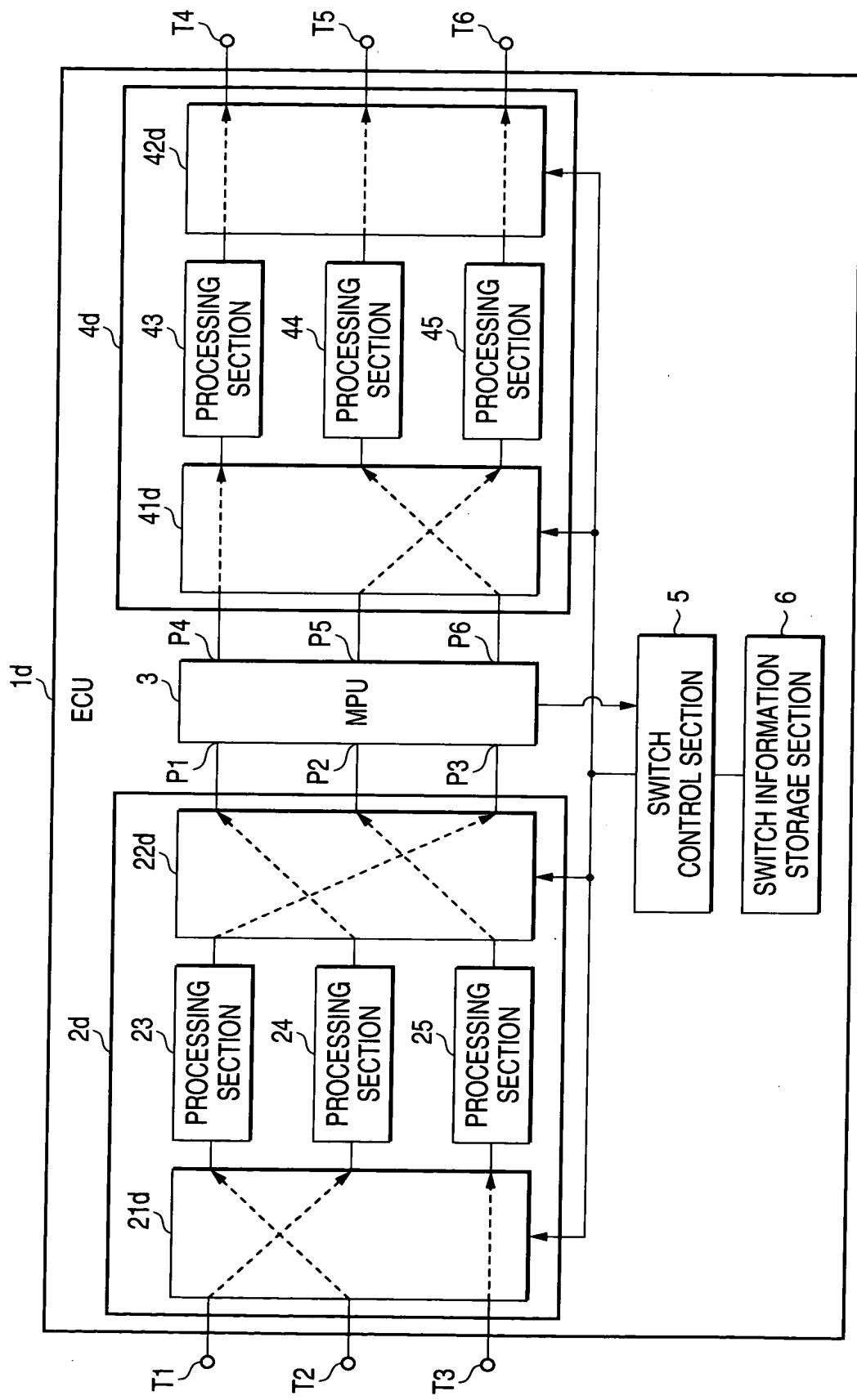


FIG. 9

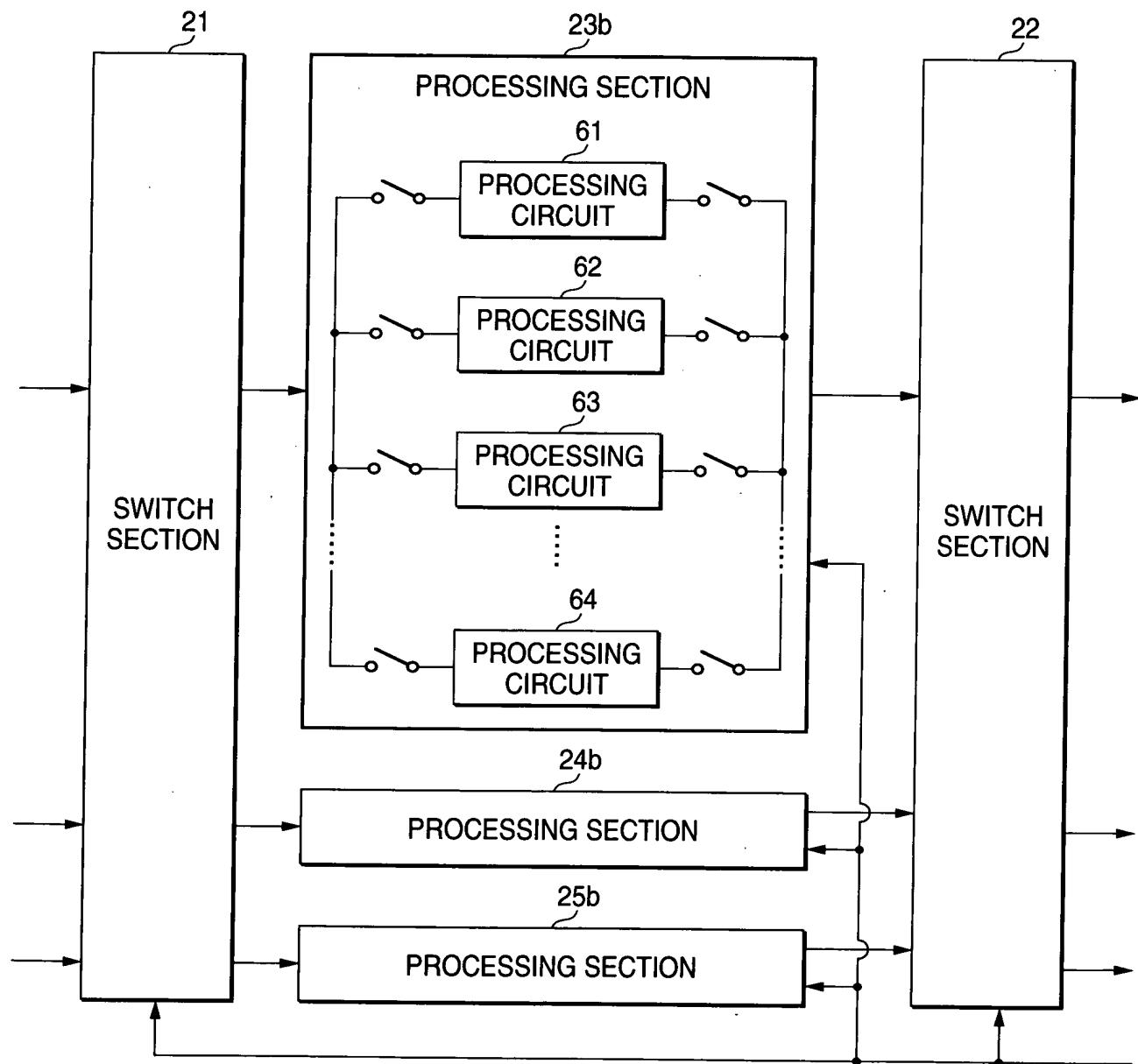


FIG. 10

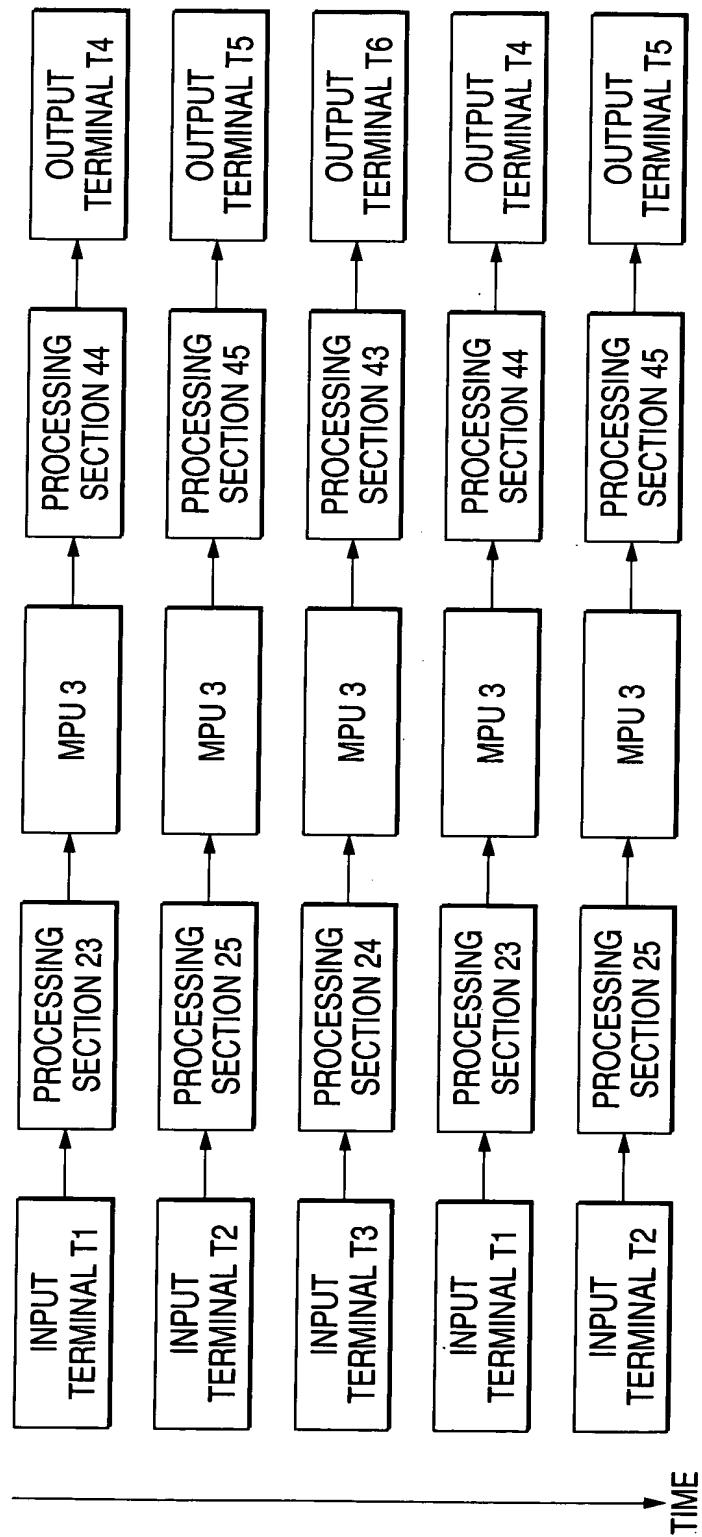


FIG. 11

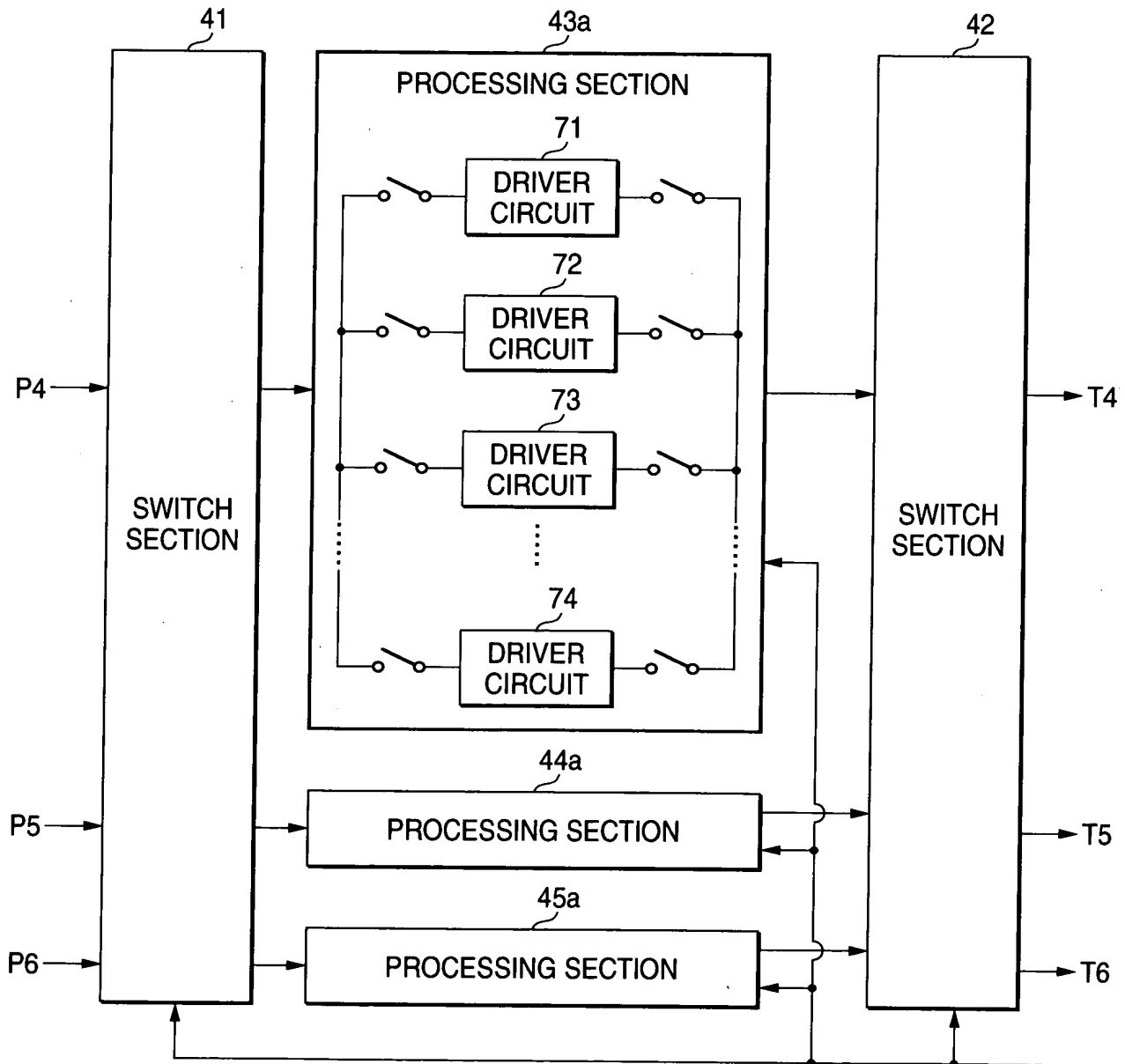


FIG. 12

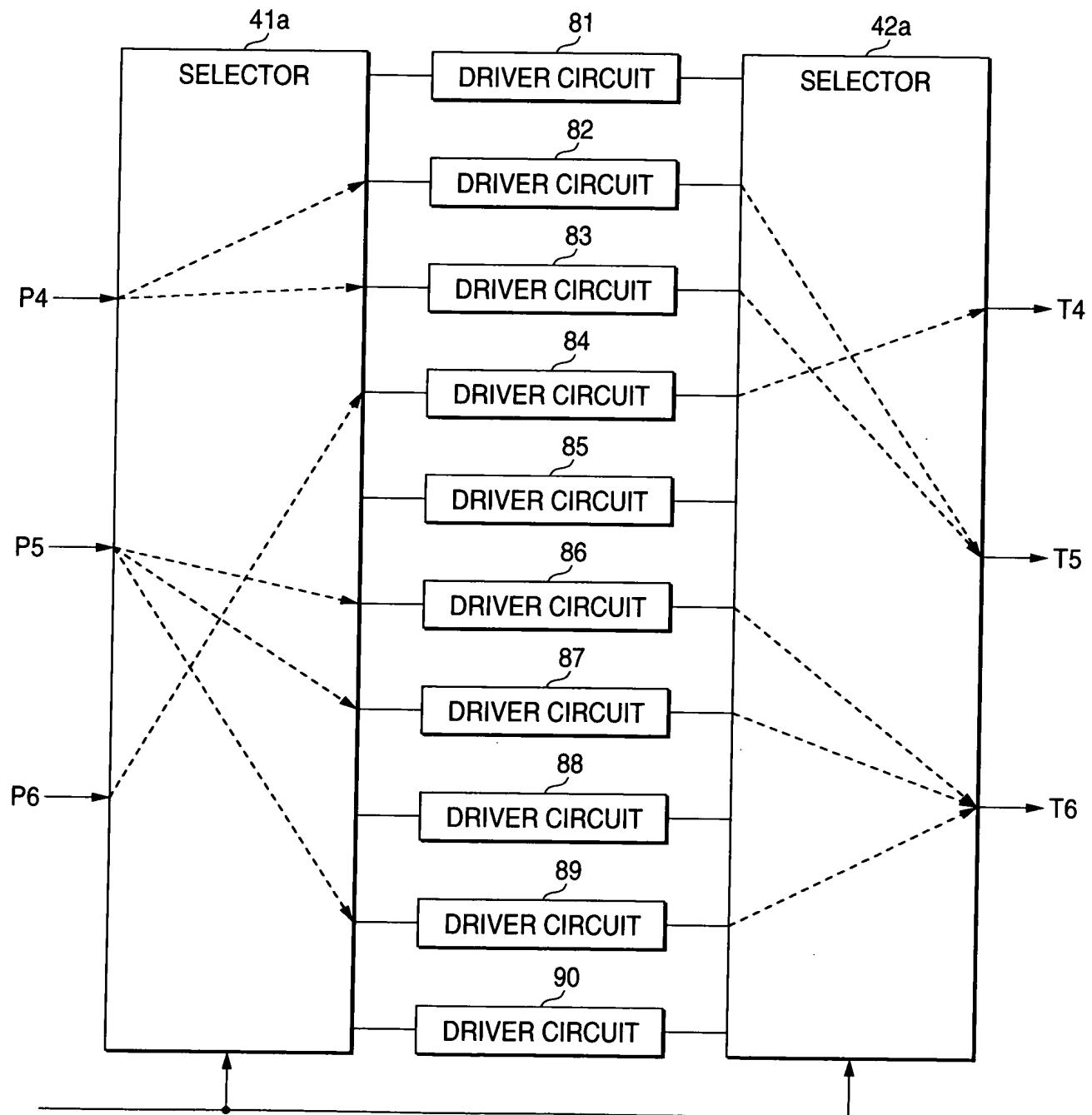


FIG. 13

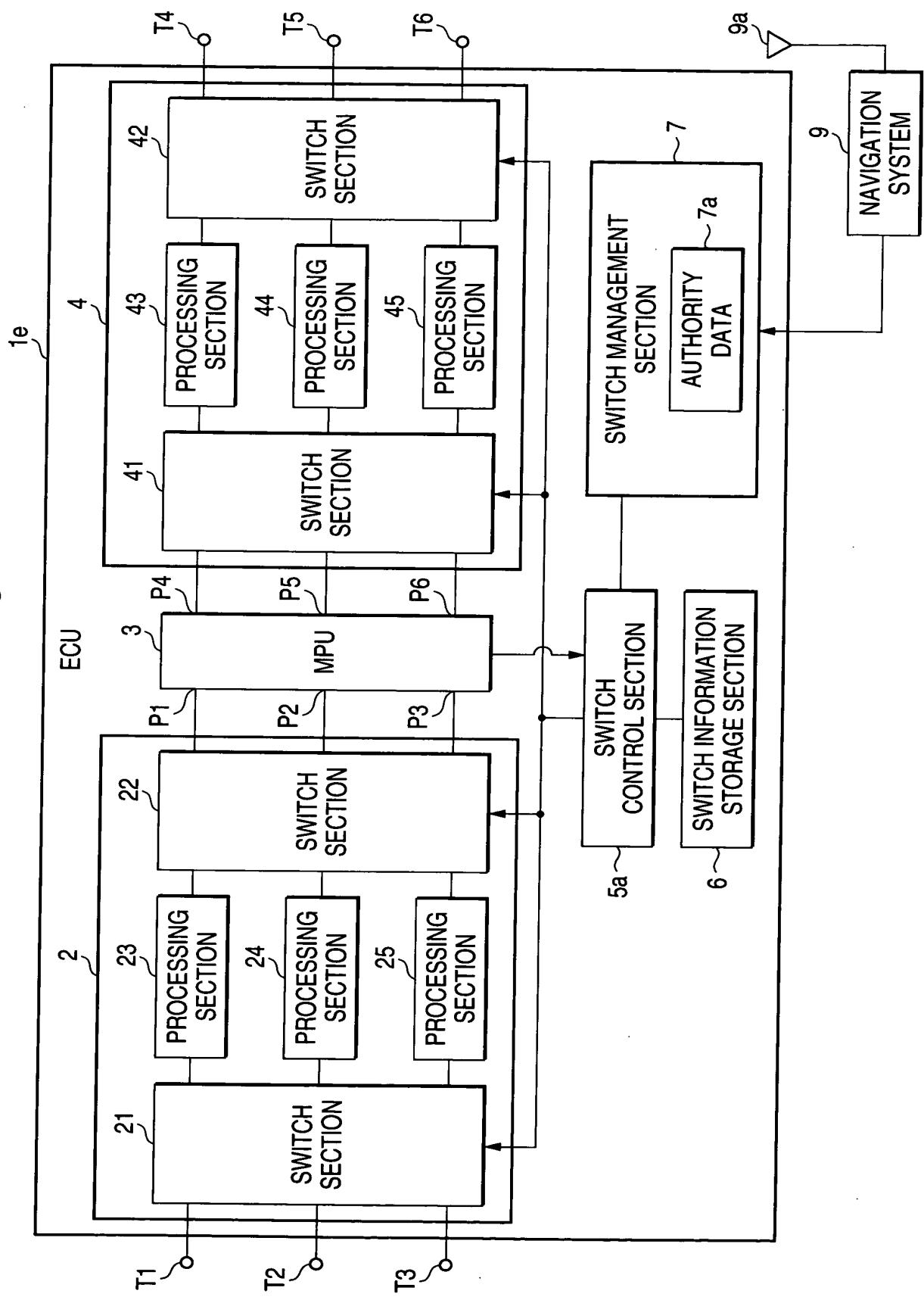


FIG. 14

	PROCESSING A	PROCESSING B	PROCESSING C	PROCESSING D
AUTHORITY LEVEL 2	PERMIT	PERMIT	PERMIT	PERMIT	
AUTHORITY LEVEL 1	PERMIT	NOT PERMITTED	NOT PERMITTED	PERMIT	
AUTHORITY LEVEL 0	NOT PERMITTED	NOT PERMITTED	NOT PERMITTED	NOT PERMITTED	

7a

FIG. 15

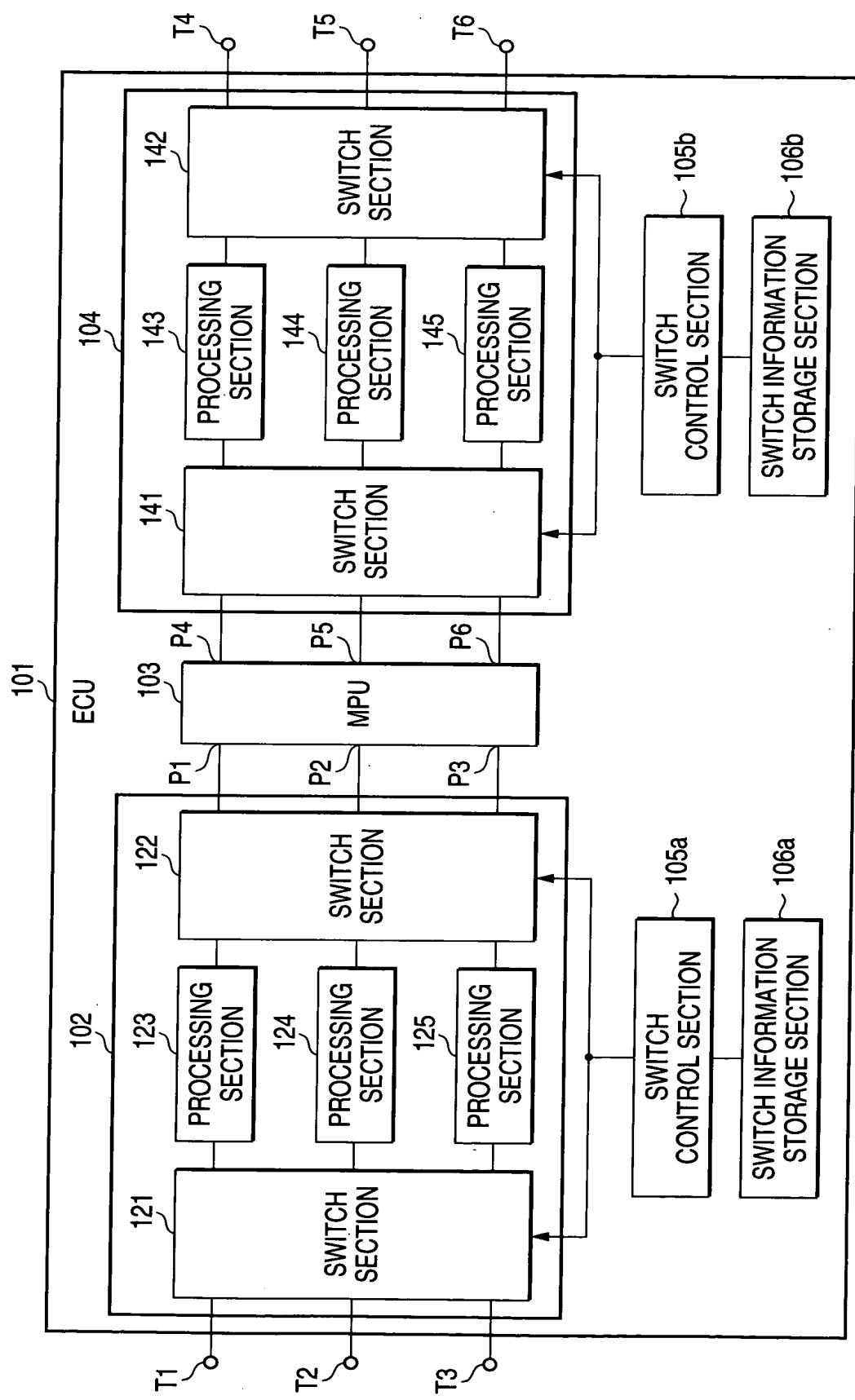


FIG. 16

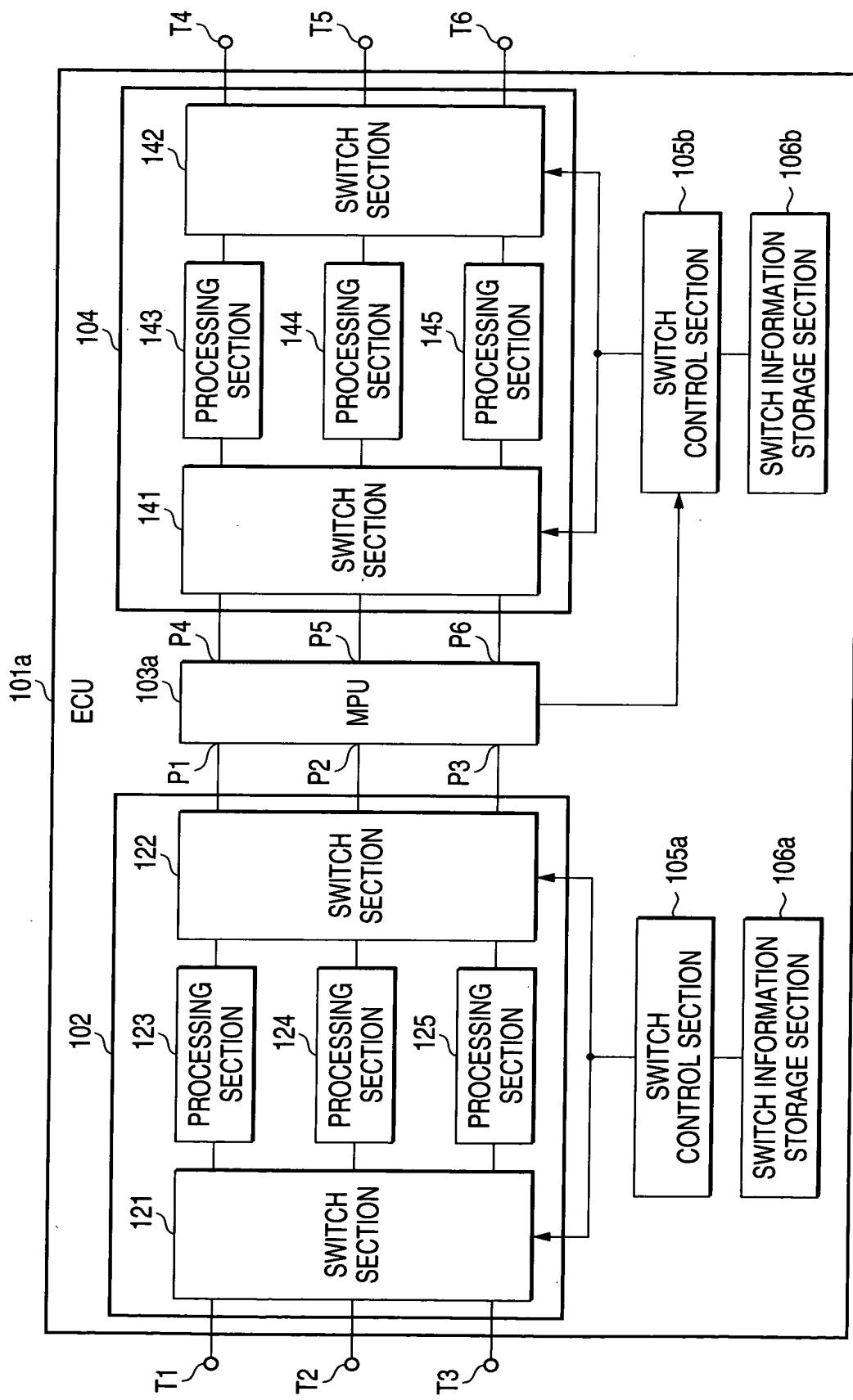


FIG. 17

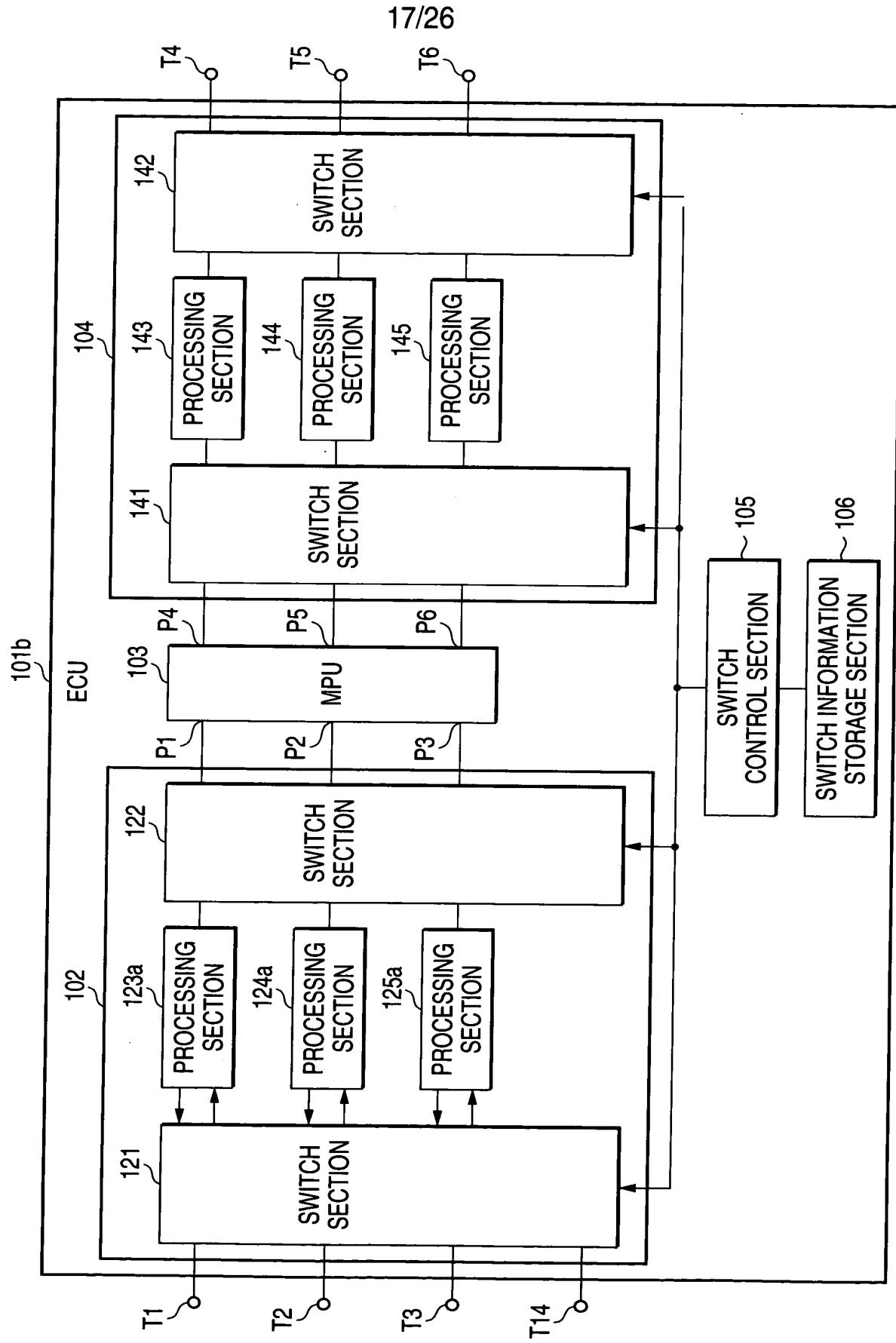


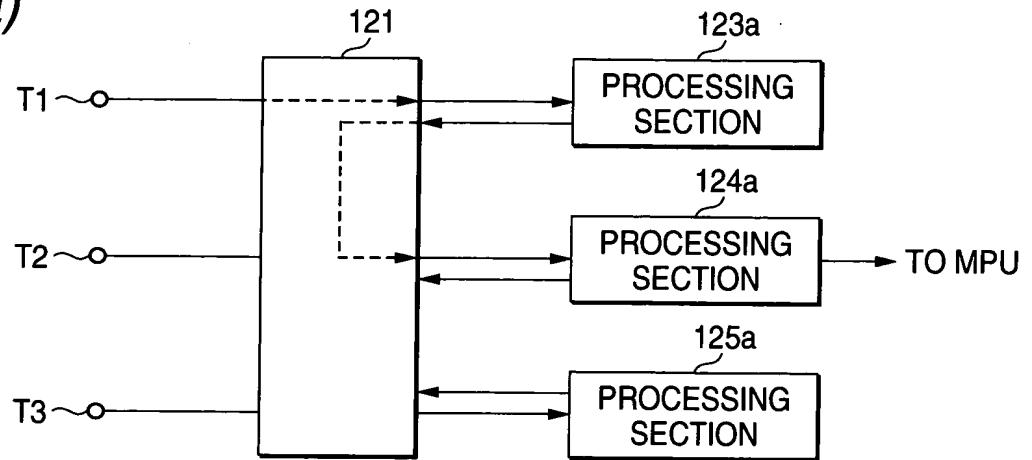
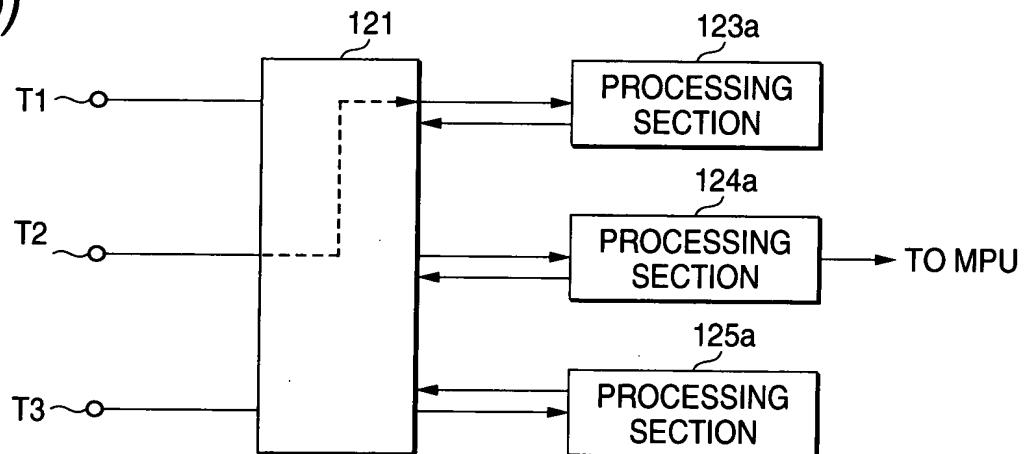
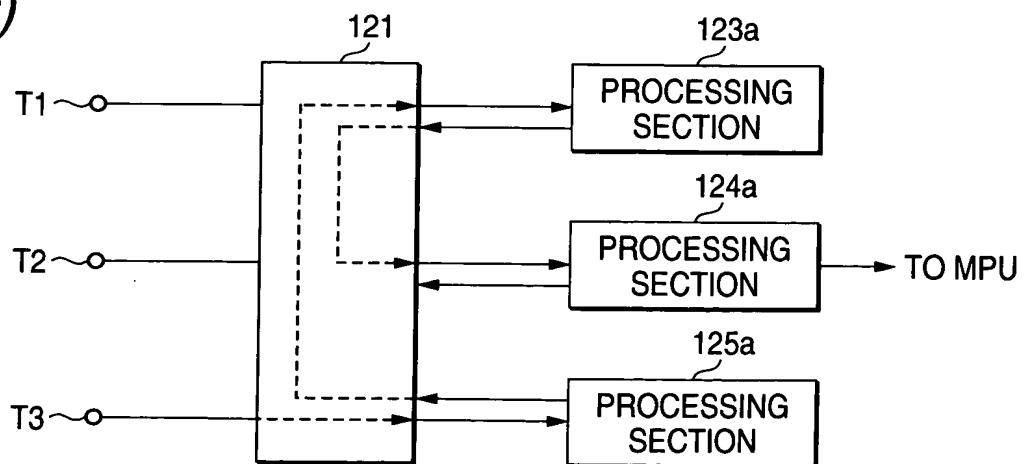
FIG. 18 (a)**FIG. 18 (b)****FIG. 18 (c)**

FIG. 19

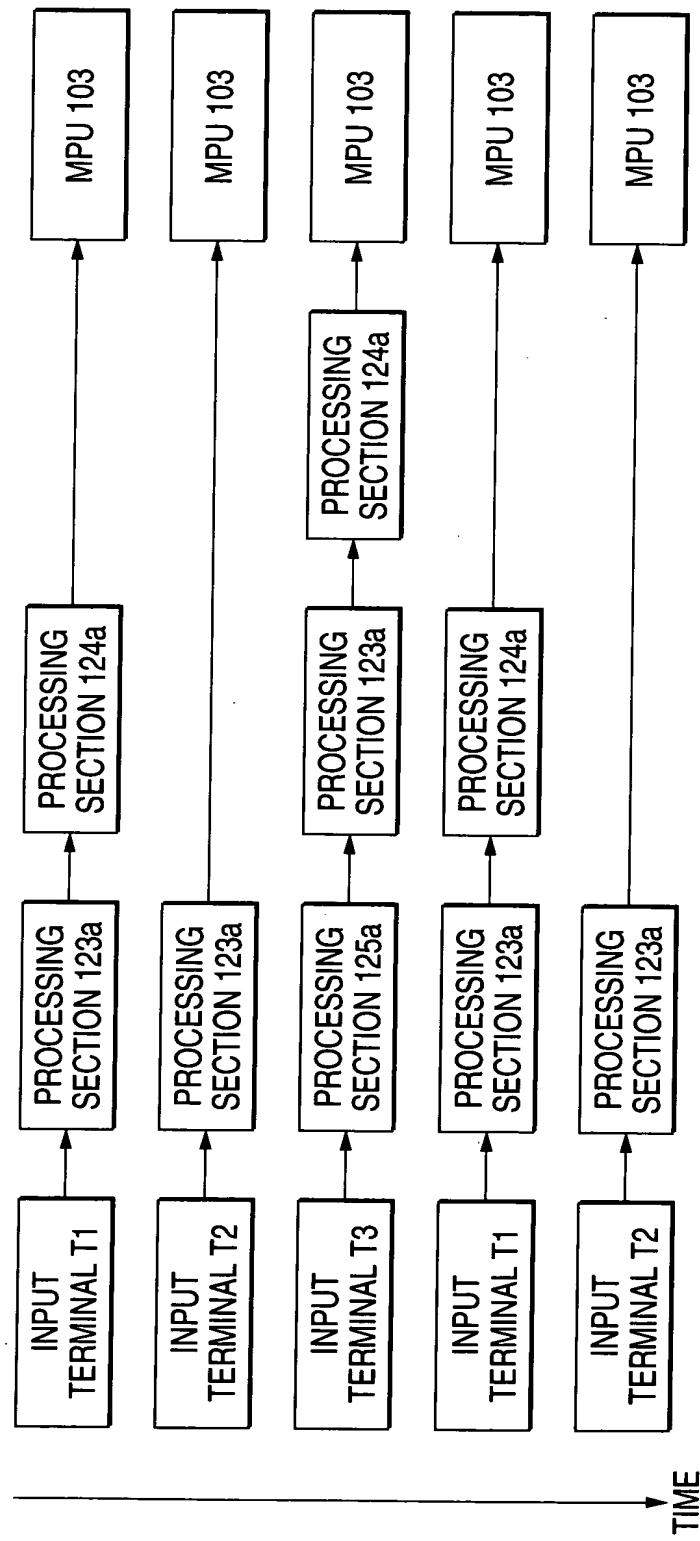


FIG. 20 (a)

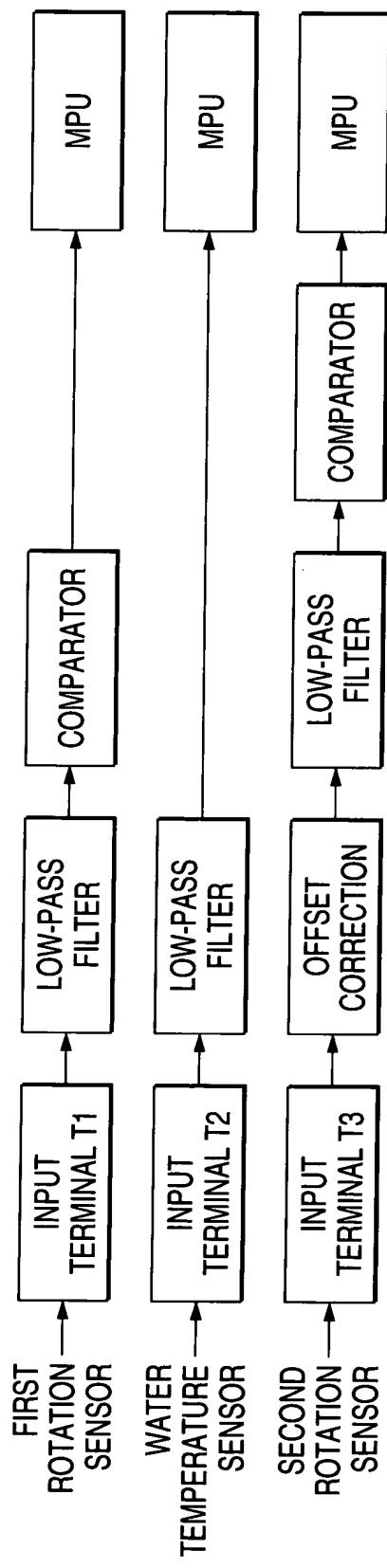


FIG. 20 (b)

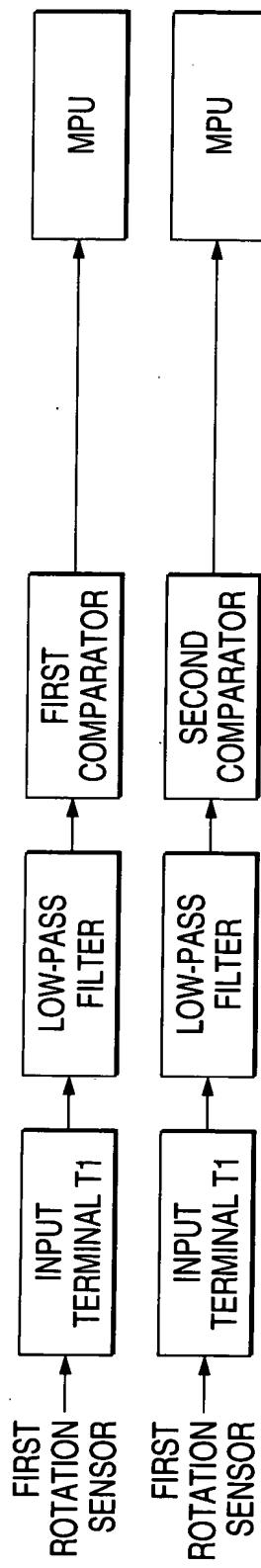


FIG. 21

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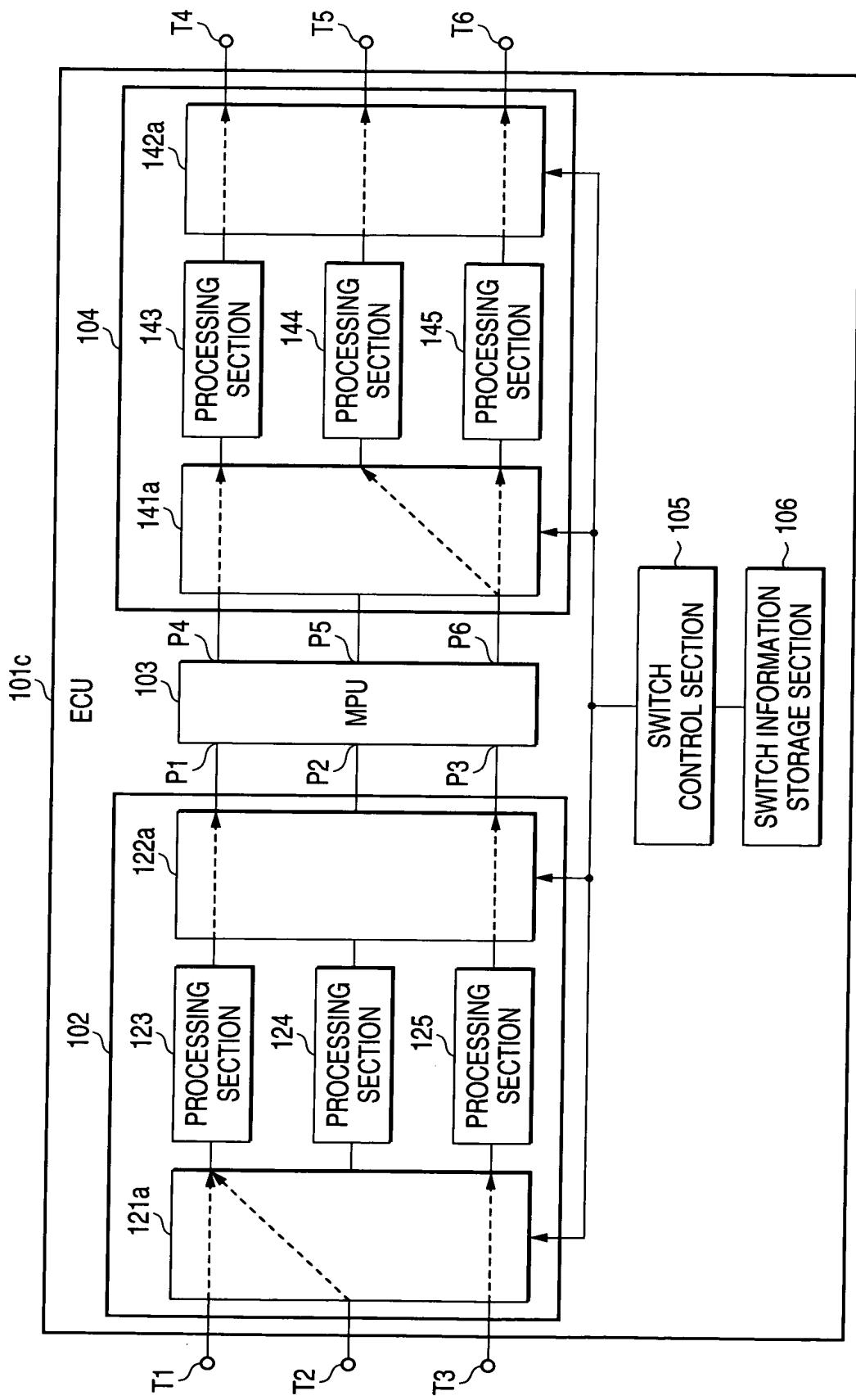


FIG. 22

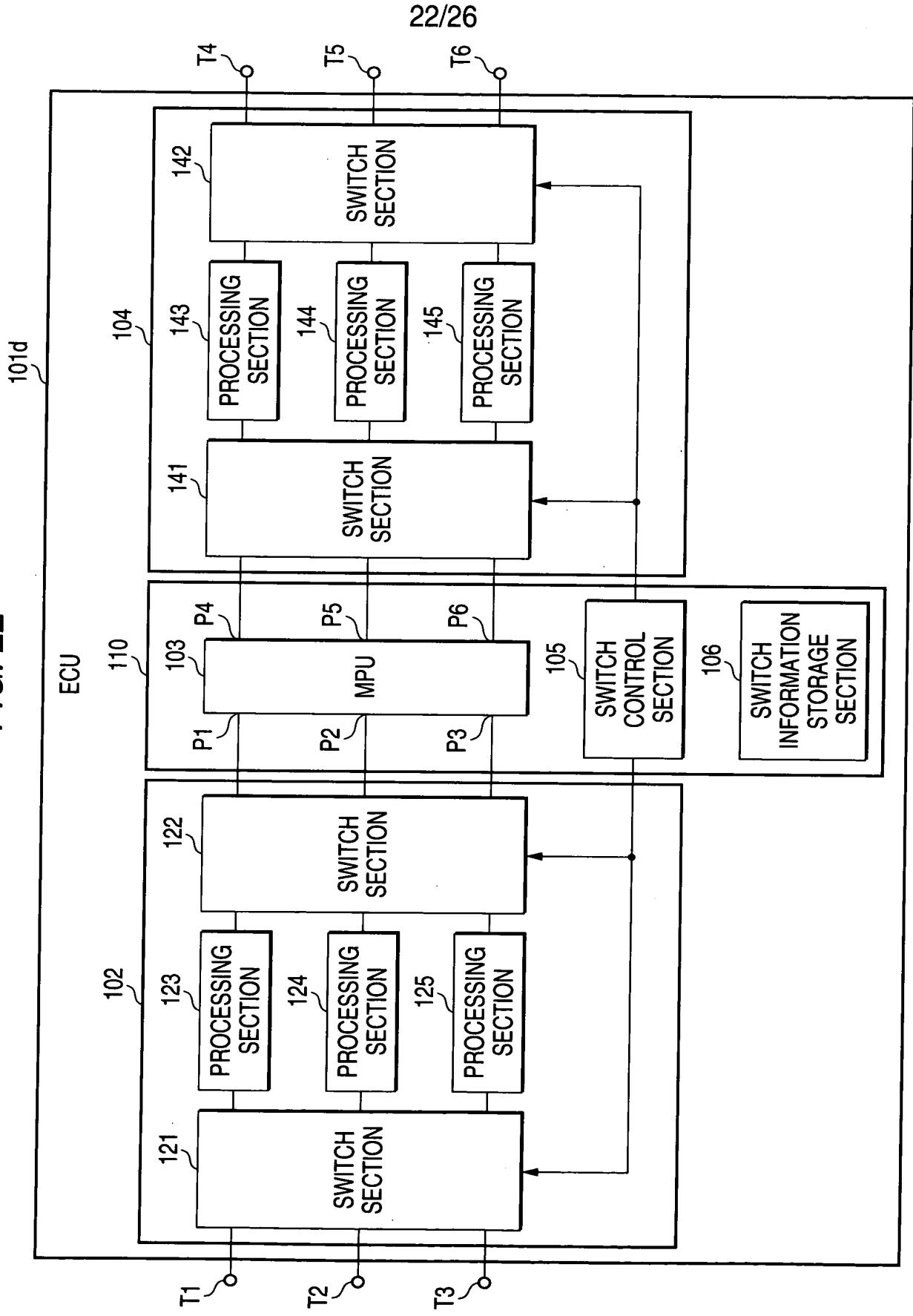


FIG. 23

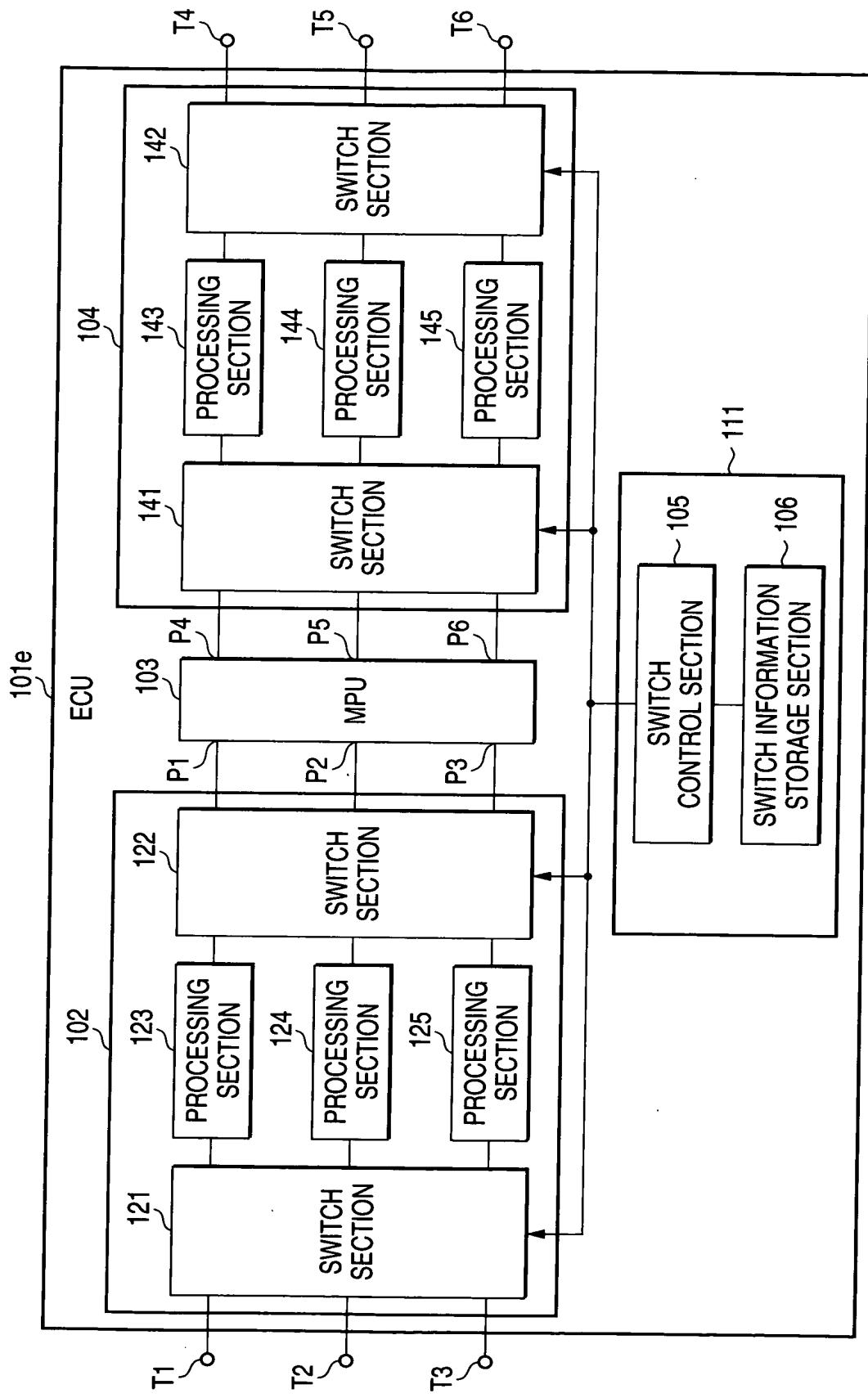


FIG. 24

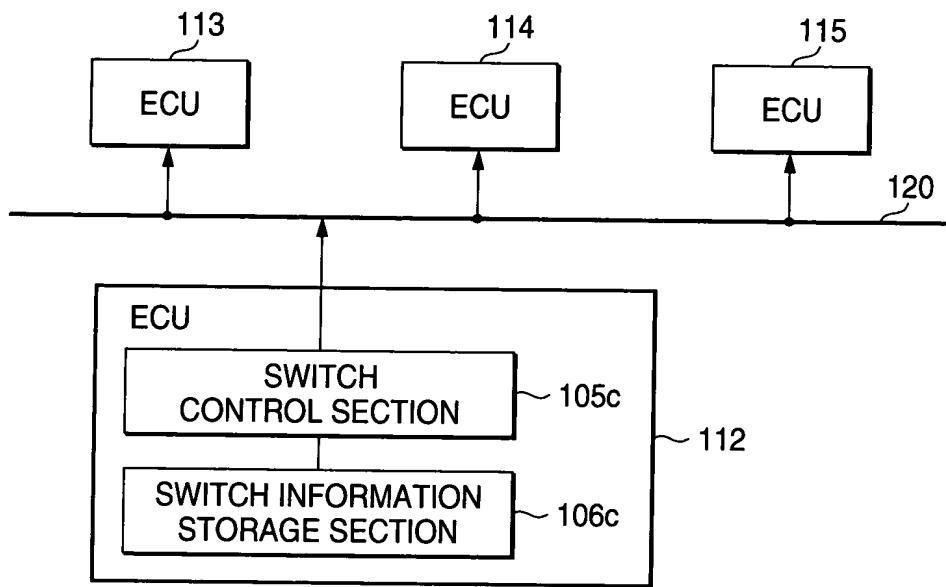


FIG. 25

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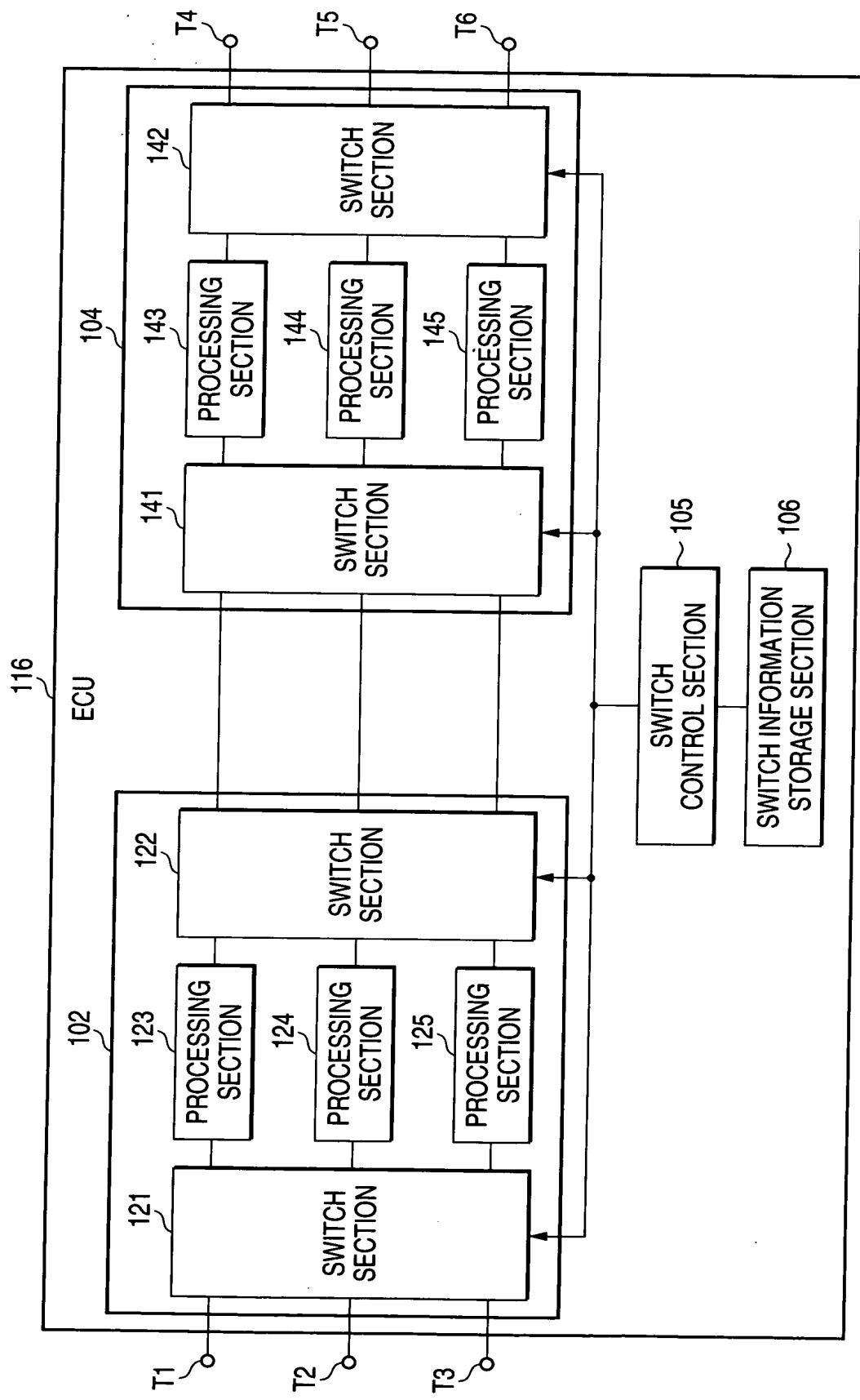


FIG. 26

